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Semi-Annual Report

Grant No. NAG-1-349

DIGITAL CONTROL SYSTEM FOR SPACE STRUCTURAL DAMPERS

Submitted to:

National Aeronautics and Space Administration Langley Research Center Hampton, Virginia 23665

> Attention: Dr. Garnett C. Horner SDD, MS 230

> > Submitted by:

J. K. Haviland Professor

₩eport No. UVA/528224/MAE84/101 January 1984

DIGITAL CONTROL SYSTEM FOR N84-16246 (NASA-CR-175355) SPACE STRUCTURAL DAMPERS Semiannual Progress Report (Virginia Univ.) CSCL 22B HC A03/MF A01

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SCHOOL OF ENGINEERING AND APPLIED SCIENCE

DEPARTMENT OF MECHANICAL AND AEROSPACE ENGINEERING

UNIVERSITY OF VIRGINIA CHARLOTTESVILLE, VIRGINIA 22901

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ABSTRACT

This is a semi-annual progress report on a study of digital control systems for space structural dampers, also referred to as "inertia" or "proof-mass" dampers. Under work performed to date, a recently developed concept for a damper has been improved by adding a small caper to the proof-mass, and using a proximeter to determine position. Also, an experimental damper has been built using a three-inch stroke in place of the standard one-inch stroke. Initially, an analog controller was used; this has now been replaced by an independent digital controller slaved to a TRS-80 Model I computer, which also serves as a highly effective, low-cost development system. An overall system concept for the use of proof-mass dampers is also presented.

SECTION I

INTRODUCTION

The active damper design which is the subject of the present study was originally proposed under NASA Grant No. NAG-1-137-1. During the period of this grant, the prototype damper shown in Figure 1 was developed, and development of the analog control system shown in Figure 2 was initiated. Under a further purchase order from NASA, No. L-46164B, the damper was redesigned as in Figures 3 and 4. Twelve of these dampers were delivered to NASA.

Under the current grant, NAG-1-349, a prototype digital ontrol system has been developed, and a prototype elongated damper has been built having a three-inch stroke as contrasted with the one-inch stroke of the original. Our current thinking on applications to large space structures is that each damper will have an individual microprocessor-driven control system whose gains can be reset by a central computer. Since it is anticipated that future space structures will experience growth during service, as new sections are added, less emphasis has been placed on optimization. It is now assumed that new dampers will be added as new structural sections are added, that these will be connected by bus to a central computer, and that adaptive control methods will be used in a central computer to change gains, or even control law programs, and to detect failures.

During this period, Mr. M. Mallette, a graduate student, has worked in parallel with the work reported here, under NASA Grant No. NGT-47-005-800.

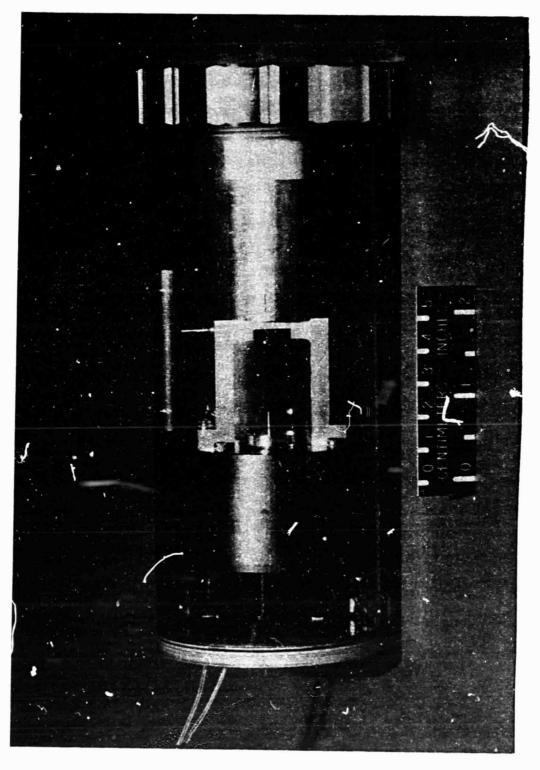
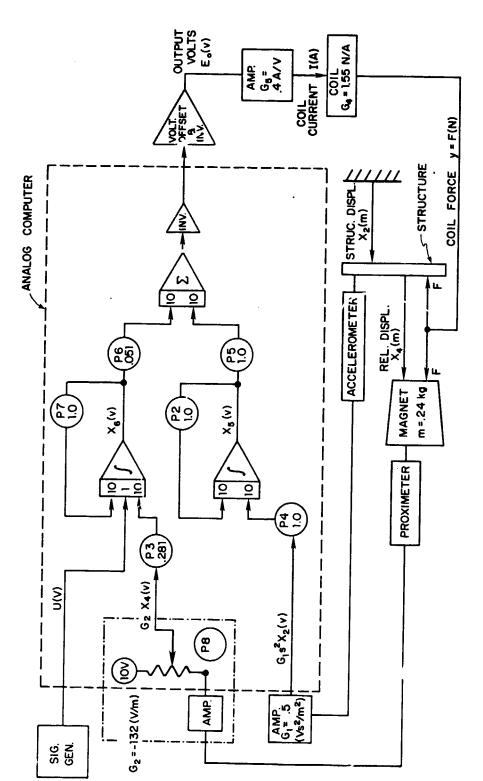


Figure 1. UVA Prototype Inertia Damper



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Figure 2. Analog Control System for Inertia Damper

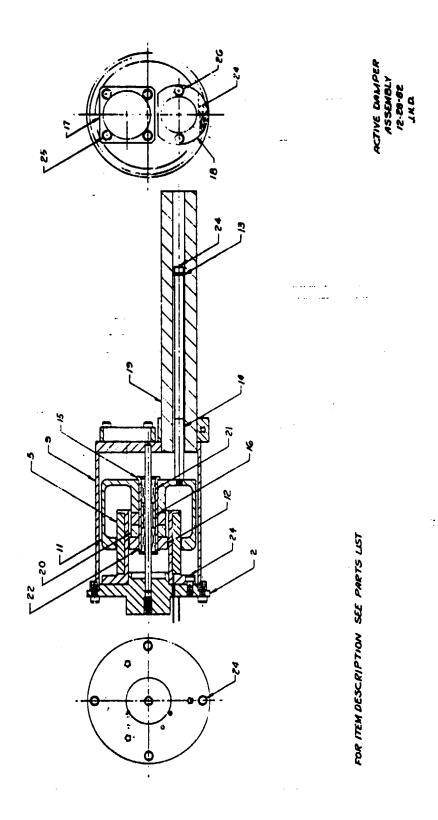


Figure 3. Section of Inertia Damper Supplied to NASA

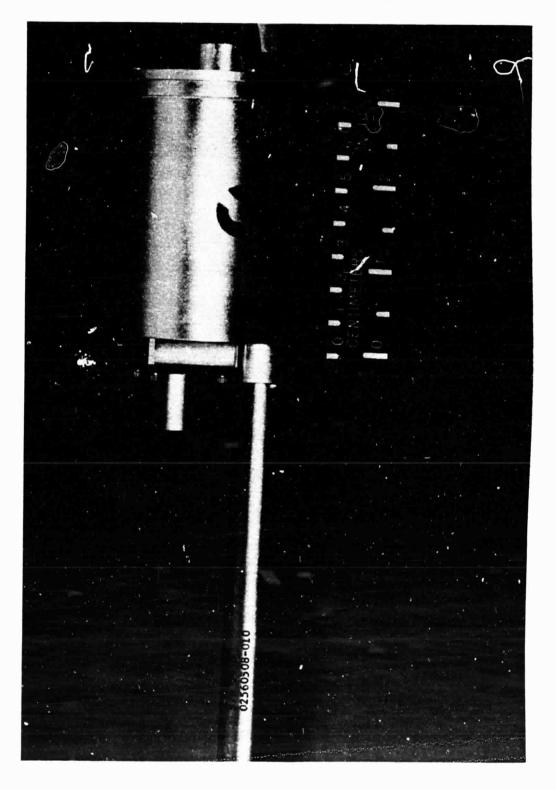


Figure 4. Inertia Damper Supplied to NASA

SECTION II

PROJECT RESULTS

Damper Design

Examples of one-inch and three-inch stroke dampers currently used in the laboratory are shown in Figures 5 and 6. Transparent covers permit their action to be observed at all times. The essential difference between these designs and the design of the dampers delivered to NASA is that the LVDT has been replaced by a proximeter. A small taper has been introduced on the proof-mass body so that its position can be determined by the proximeter.

Analog Control Circuit

The analog control circuit, as finally developed, is shown in Figure 2. Values shown for gains were selected during tests, with the actuator attached to a 15 ft. beam. Equations developed for this circuit are shown in Figure 7; these feature the three transfer functions H_1 , H_2 and H_3 , which represent coil force due to inputs from the accelerometer, the proximeter, and a signal generator, respectively. The latter is used for testing the system.

A block diagram for the complete system is shown in Figure 8. From this, the equations of Figure 9 were developed. The transfer function $H_{\mathbf{c}}$ is the complex damping coefficient, which limits to the design damping coefficient c at high frequencies.

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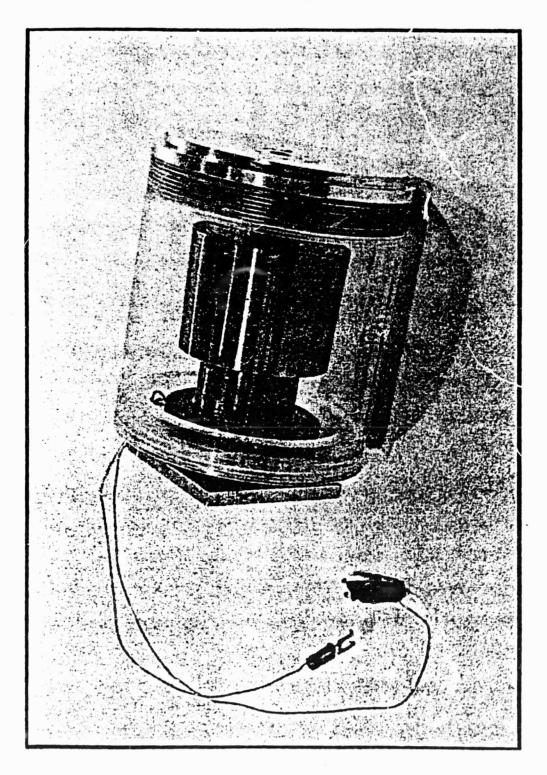


Figure 5. Modified Prototype Damper, One-Inch Stroke

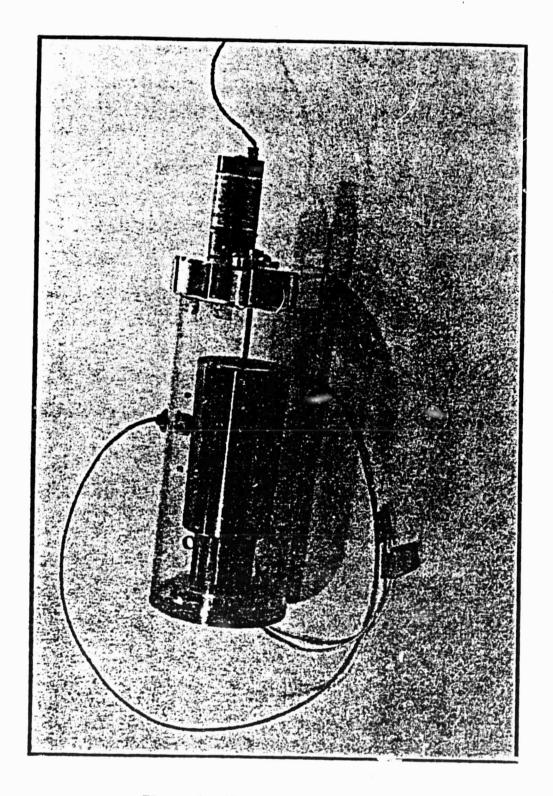


Figure 6. Three-Inch Damper Prototype

Definitions

 $x_1 = Structural velocity (m/s)$

 $x_2 = Structural deflection (m)$

 x_3 = Proof mass velocity (m/s)

 \mathbf{x}_{L} = Proof mass relative displacement (m)

 $x_5 = Integrator output (v)$

 $x_6 = Integrator output (v)$

 $E_{O} = Output volts (v)$

I = Output current (A)

F = y = Coil force (N)

m = Proof mass (m)

 $G_1 = Gain of accelerometer (Vs²/m)$

 $G_2 = Gain of proximeter (v/m)$

 G_{L} = Coil force for unit current (N/A)

 $G_5 = Gain of coil driver (A/V)$

u = Input signal (v)

Equations

$$F = y = H_1 x_2 + H_2 x_4 + H_3 u$$
 (N)

$$F/ms^2 = x_2 + x_4 (m)$$

$$H_1 = \frac{100 \text{ G}_1 \text{G}_4 \text{G}_5 \text{P}_4 \text{P}_5 \text{s}^2}{\text{s} + 10 \text{ P}_2} = \frac{\text{cs}^2}{\text{s} + \omega_a} \qquad (\text{N/m})$$

C = Design damping coefficient (Ns/m)

Figure 7. Analog Circuit Summary

Equations (continued)

 $\omega_{\rm g} = \text{Roll-off frequency for accelerometer (s}^{-1}$)

$$H_2 = \frac{100 G_2 G_4 G_5 P_3 P_6}{s + 10 P_7} = -\frac{k \omega_p}{s + \omega_p} \qquad (N/m)$$

k = Design stiffness (N/m)

 $\omega_p = \text{Roll-off frequency for proximeter (s}^{-1})$

$$H_3 = \frac{10 \text{ G}_4 \text{G}_5 \text{P}_6}{\text{s} + 10 \text{ P}_7} = \frac{\text{F}_0 \omega_p}{\text{s} + \omega_p} \qquad (\text{N/V})$$

 $F_{O} = \text{Coil Force for Unit Signal Generator Voltage (N/V)}$

Typical Values

$$G_{1} = 0.5 \text{ (Vs}^{2}/\text{m)}; \qquad G_{2} = -132 \text{ (V/m)}$$

$$G_{4} = 0.4 \text{ (V/A)}; \qquad G_{5} = 1.55 \text{ (N/A)}$$

$$H_{1} = \frac{31s^{2}}{s+10} \text{ (N/m)}; \qquad C = 31 \text{ (Ns/m)}$$

$$\omega_{a} = 10(s^{-1})$$

$$H_{2} = \frac{-117}{s+10} \text{ (N/m)}; \qquad k = 11.7 \text{ (N/m)}$$

$$\omega_{p} = 10(s^{-1})$$

$$H_{3} = \frac{0.316}{s+10} \text{ (N/v)}; \qquad F_{0} = 0.0316 \text{ (N/V)}$$

Figure 7. Analog Circuit Summary (Continued)

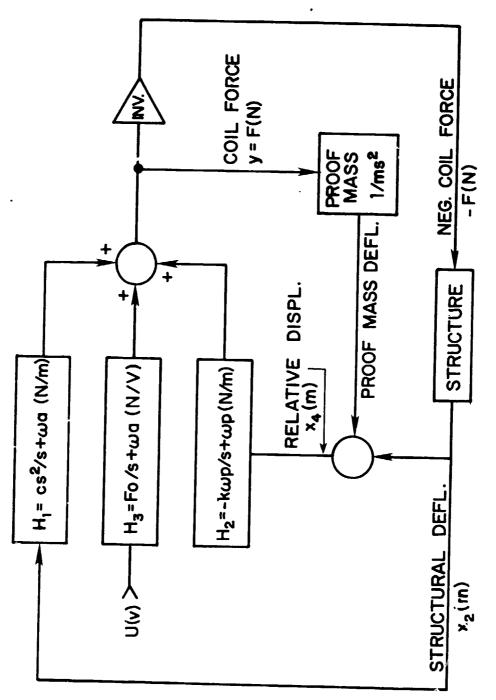


Figure 8. Block Diagram of Analog Circuit

Given:

$$F = H_1 x_2 + H_2 x_4 + h_3 u \qquad (N)$$

$$F = ms^2 (x_4 + x_2) \qquad (N)$$

$$F = \frac{H_1 - H_2}{1 - H_2 / ms^2} x_2 + \frac{H_3}{1 - H_2 / ms^2} u = H_c s x_2 + H_u u \qquad (N)$$

$$H_c = \frac{cs^3 (s + \omega_p) + k \omega_p s (s + \omega_a)}{s^2 (s + \omega_a) (s + \omega_p) + k \omega_p (s + \omega_a) / m} \qquad (Ns/m)$$

= True damping coefficient

Figure 9. Analysis of Block Diagram for Analog Circuit

Digital Control Circuit

The digital control circuit now under development is shown in Figure 10. Input signals are converted to the range 0-5 V, digitized to one-byte values, and read into a TRS-80 Model I computer. Output from the computer is reconverted to a 0-5 V signal, and is used to drive a NASA developed current amplifier which drives the coil. Equations developed for this system are shown in Figure 11.

Values for the constants in the expression for H_1 , H_2 have the same values as those in Figure 7 when the appropriate values for G_a , G_ρ , ω_a , ω_ρ are used in the digital computer program. However, as supplied to the computer program listed in Figure 12, they are in the form G_a T, etc., where T is the sampling time interval, set at 2 ms.

Keyboard inputs permit these values to be increased or decreased by factors of two, thus affording some measure of external control over the parameters. This feature was added to the program to demonstrate a particular advantage of a digital system, namely, that is permits gains to be reset by remote control.

The digital control described above was demonstrated at the Langely Laboratories of NASA in August 1983. A unique feature of this controller is that it incorporates a development system using a relatively cheap home computer. Competitive systems use costly development systems purchased from the manufacturer of the microchip.

Current Development of Digital Control Circuit

During ongoing work, a Z80 microchip and 4K of RAM memory have been incorporated into the control box, the Z80 being slaved to the TRS-80 Model I computer. A simple modification to the computer has reduced

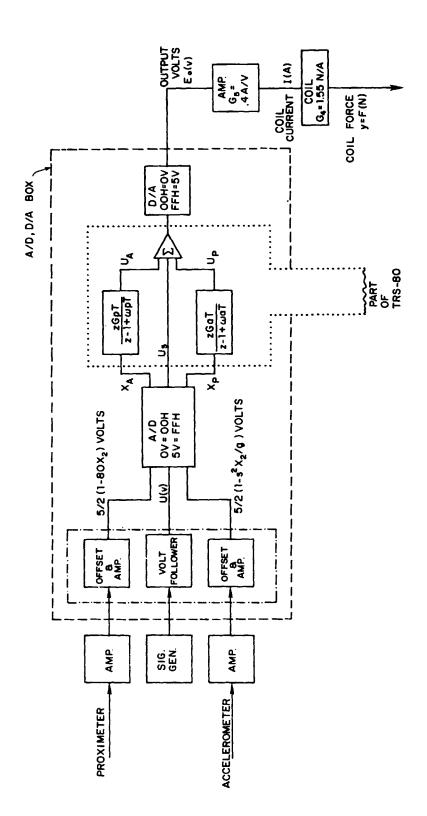


Figure 10. Digital Control System

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$$H_1 \sim \frac{0.158 \text{ G}_A}{\text{s} + \omega_A} \text{ s}^2 = \frac{\text{cs}^2}{\text{s} + \omega_A}$$
 (N/m)

$$H_2 \sim -\frac{124Gp}{s + \omega_p} = -\frac{k\omega_p}{s + \omega_p}$$
 (N/m)

$$H_3 = 0.62$$
 (N/v)

for typical values

$$\omega_{a} = 10(s^{-1}),$$
 $\omega_{p} = 10(s^{-1})$
 $c = 31 \text{ (Ns/m)},$ $G_{a} = 196,$

$$k = 11.7 (N/m) = 0.237 lb/in, Gp = 0.94$$

Digital Equations (Simple Integration)

$$u_{a_{i+1}} = u_{a_{i}} (1 - \omega_{a}T) + G_{a}Tx_{a_{i}}$$

$$u_{a_{i+1}} = u_{p_{i}} (1 - \omega_{p}T) + G_{p}Tx_{p_{i}}$$

$$\Sigma = u_{a_{i}} + u_{p_{i}} + u_{s_{i}}$$

Figure 11. Analysis of Digital Control Gains

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```
99199
         ORG
               7000H
00110 SERVOI DI
         CALL 01C9H
00120
00130
         LD
              C,20H ;SET T=2MS
00140
         LD
             IX,7400H
00150
         LD
              (IX).5
00160
        LD
             6,(1XXI)
00170
        LD
              (IX+2),2
        LD
99189
              (IX+3),9
        LD
00190
              HL,0
                         ;INIT ACCEL.
         EXX
00200
         LD
              HL,0
00210
                         ;INIT. PROX.
00220
         EXX
         CALL DISOTA
00230
         CALL DISOTP
60240
00250
         CALL DISGTA
00260
         CALL DISGTP
00270 TIME IN
               A,(0) ; READ STATUS
         AND C
00280
                   TEST FOR TIME
         JP Z,TIME ;RETURN IF LESS
00290
00291
         PUSH BC
        IN A,(20H) ; RESET A/D C; OCK
00300
         OUT (20H),A
003i0
00320
        LD
              B.(IX)
00330
         CALL STEP
00340
         CALL READ
         NEG
00350
00360
         LD
              B,(IX+2)
00370
        CALL INTEG
        EXX
00380
00390
         OUT
              (21H),A ;START PROX.
99499
        LD
             B,(IX+1)
00410
         CALL STEP ;SUB. OTP*UP(I-1)
00420
        CALL READ ; READ PROX.
         LD
00430
              B,(IX+3)
         CALL INTEG ;ADD GTA*PROX.
00440
        PUSH HL
00450
                    ;XFER. UP
00460
         OUT
              (22H), A ; START SIG.
00470
         ĒΧΧ
00480
         LD
              B,H
                   ;SAVE
00490
         LD
              C,L
                    ;UA
        POP
00500
              DΕ
                    GET UP
99519
         OR
               Α
         ADC
00520
              HL,DE ;ADD UP
         CALL OVER
99539
00540
         CALL READ ; READ SIG.
              D,A
         LD
                    ;SIG.
99559
         LD
              Ε,θ
                   ;INTO DE
00560
         OR
00570
               Α
         ADC
              HL,DE ;ADD SIG.
00580
00590
         CALL OVER
```

Figure 12. Control Law Program in Z80 Machine Language

```
01140 TEST3 CP
                 33H
         JP
             NZ,TEST4
01150
01160
         CALL INGTA
01170
         RET
01180 TEST4 CP
                 34H
         JP
             NZ,TESTO
01190
01200
         CALL INGTP
01210
         RET
01220 TESTO CP
                  4FH
         JP
               NZ,TESTW
01230
01240
         CALL DEOTA
01250
         RET
01260 TESTW CP
                  57H
         JP
             NZ,TESTG
01270
         CALL DEOTP
01280
01290
         RET
01300 TESTG CP
                 47H
         JP
               NZ,TESTP
01310
         CALL DEGTA
01320
01330
         RET
01340 TESTP CP
                 50H
         JP
01350
              NZ,RET
01360
         CALL DEGTP
01370 RET RET
01380 INOTA INC
                  (IX)
         CALL DISOTA
01390
         RET
01466
01410 INOTP INC (IX+1)
01420
         CALL DISOTP
         RET
01430
01440 INGTA INC
                 (IX+2)
01450
         CALL DISGTA
01460
         RET
01470 INGTP INC
                  (IX+3)
01480
         CALL DISGTP
01490
         RET
01500 DEOTA DEC (IX)
01510
         CALL DISOTA
01520
         RET
01530 DEOTP DEC (IX+1)
01540
         CALL DISOTP
01550
         RET
01560 DEGTA DEC
                 (IX+2)
01570
         CALL DISGTA
01580
         RET
01590 DEGTP DEC
                  (IX+3)
91600
         CALL DISGTP
         RET
01610
01620 DISOTA LD
                  A,(IX)
01630
         AND
                0FH
91649
         ADD
               A,30H
01650
         LD
               (3C48H),A
01660
         RET
01670 DISOTP LD
                 A,(IX+1)
```

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Figure 12. Control Law Program in Z80 Machine Language (continued)

01680	AND	0FH	
01690	ADD	A,3 0 H	ORIGINAL PAGE IS
01700	LD	(3C88H),A	OF POOR QUALITY
01710	RET		en Court
91729 DI	ISGTA LI) A,(IX+2)	
01730	AND	0FH	
01740	ADD	A,30H	
01750	LD	(3CC8H),A	
01760	RET		
01770 DI	SGTP LD	(E+XI),A (
01780	AND	0FH	
01790	ADD	H0E,A	
01800	LD	(3D08H),A	
01310	ret		
01820	END	SERVO1	

Figure 12. Control Law Program in Z80 Machine Language (continued)

```
00600
          LD
                A,H
                      :HIGH BYTE OF Y
00610
          ADD
                 A,80H ;CONV. FOR OUTPUT
00620
          OUT
                (10H),A ;OUTPUT Y
00630
          LD
                H,B
                     ;REPLACE
00640
          LD
                L,C
                     ;UA
00641
          POP
                BC
00650
          CALL KEY
                A,(3840H);READ KEYBOARD LINE
00660
          LD
99679
          CP
                    ;TEST FOR BREAK
00680
          JF
               NZ,TIME ;CONT.
00690
          RST
                40
99799 READ IN
                  A,(0) :READ STATUS
          AND
                 80H
                       ;TEST EOC
00710
00720
          JP
                Z,READ ;RETURN IF LOW
                A,(10H); READ A/D
00730
          IN
99749
          ADD
                 A,80H
09750
          RET
00760 STEP
            LD
                  D,H
                        ;U
00770
          LD
                E,L
                     ;INTO DE
00780
          CALL SHIFT ; INIT. SHIFT
00790
          OR
                Α
96899
          SBC
                HL,DE ;SUB OT*U(I-1)
00810
          CALL OVER
00820
          RET
00830 INTEG LD
                  D,A
                         įΕ
                E,0
00840
          LD
                      ;INTO DE
00850
          CALL SHIFT ; INIT. SHIFT
99869
          OR
                Α
00870
          ADC
                HL,DE ;ADD GT*E
00880
          CALL
                OVER
00890
          RET
00700 SHIFT SRA
                   D
                        ;RT. SHIFT D
00910
          RR
                Ε
                     ;RT. ROT. E
00920
          DEC
                В
00930
          JP
                NZ,SHIFT
                            CONT. UNTIL B CLEARS
00940
          RET
             JP
                  PO,CONT
00950 GVER
          JP
00750
                C,MINUS
00970
          LD
                HL,7FFFH
00980
          JP
                CONT
00990 MINUS LD
                   HL,8000H
01000 CONT
            RET
01010 KEY
            CALL
                  2BH
01020
          CP
01030
          JP
                NZ,PRINT
          RET >
01040
01050 PRINT LD
                  (3C00H),A
01060 TESTI CP
                  31H
01070
          JP
                NZ.TEST2
01080
          CALL INOTA
01070
          RET
01100 TEST2 CP
                  32H
01110
          JP
                NZ,TEST3
          CALL
01120
               INOTP
01130
          RET
```

Figure 12. Control Law Program in Z80 Machine Language (continued)

internal RAM memory from 48K to 32K, leaving a "hole" in internally decoded memory of 16K. When the control box is attached to the bus, its 4K memory becomes mapped into the high address memory of the TRS-80, so that the control program can be loaded. Appropriate output codes can disconnect this memory and start the Z80, which then runs the control program independently of the TRS-80.

Capabilities of this system include the following:

- 1. Ability to run as an independent controller,
- 2. Ability to receive gain changes from the TRS-80,
- 3. Ability to load new control programs from the TRS-80,
- 4. Usefulness as a development system for control programs, and
- 5. One 2K RAM can be replaced by an EPROM, so that the TRS-80 will not be required for start-up.

SECTION III

SYSTEM CONSIDERATIONS

Our original conception was that considerable emphasis must be placed on determining optimum locations for dampers. However, it now seems to be evident that the typical large space structure will undergo considerable modifications and additions during its life, so that optimization of damper locations for any given configuration makes little sense.

Our present concept is that a general purpose damper should be developed, controlled by an individual digital system, whose control law can be dictated by a central computer. Under such a system, the only fixed parameters would be the value of the proof mass and its permissible double amplitude. Given these constraints, the permissible damping factor c can be determined for any given structural amplitude and frequency. Thus assuming a control law which rolls off suitably at low frequencies, the permissible structural amplitude should be only slightly less than the permissible double amplitude of motion of the proof mass.

Following this thinking, we intend to emphasize the development of more sophisticated control laws, paying special attention to the reduction of resonance peaks now present. We also intend to investigate the consequences of "bimping," i.e., of allowing the proof mass to strike the stops. In particular, we want to be sure that no limit cycle motions are possible, in which the proof mass repeatedly strikes the stops.

Figure 13 shows the hypothetical control configuration for a large space structure in which the inertial (or proof-mass) dampers are individually controlled, but are connected to a central computer, so that they can be reprogrammed as required.

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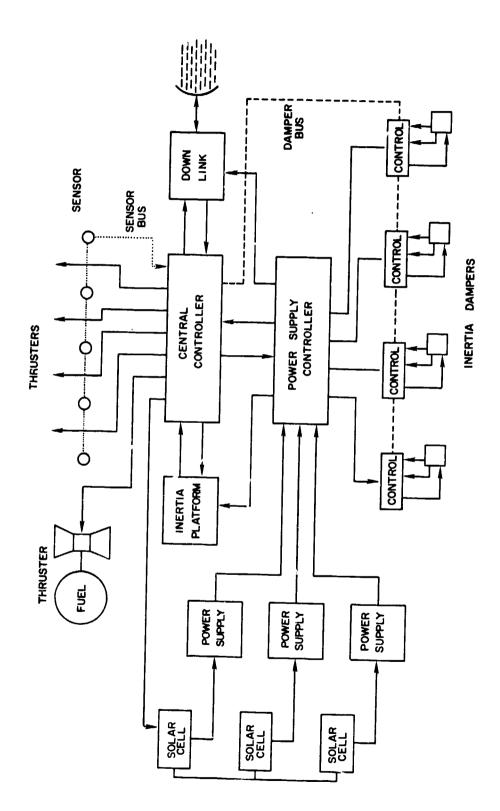


Figure 13. Hypothetical Control Configuration for Large Space Structure with Dampers

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SECTION IV

PLANS FOR REMAINDER OF PERIOD

During the remainder of this period, the adapter box, presently containing wire-wrapped A/D and D/A convertors, will be modified by installing a Z80 microprocessor and associated memory. This will demonstrate the concept of the individual damper which can be reprogrammed from a central computer (the Radio Shack TRS-80 Model I in this case).

At the same time, work on development of improved control laws will continue. This work will constitute part of the doctoral dissertation to be presented by Mr. Mallette.